Name of Institute: Indus Institute of Technology & Engineering
Name of Faculty: Prof. Zalak Patel

Course code: EC0422
Course name: Modern Communication Systems
Pre-requisites: Analog Communication, Digital Communication
Credit points: 03
Offered Semester: 4th

Course Coordinator (weeks 15)
Full Name: Prof. Zalak Patel
Department with sitting location: EC (Antenna & Microwave Lab), Bhanwar Building
Telephone: 3203
Email: zalakpatel.ec@indusuni.ac.in
Consultation times: 3:30 to 4:15 PM

Course Lecturer (weeks 15)
Full Name: Prof. Zalak Patel
Department with sitting location: EC (Antenna & Microwave Lab), Bhanwar Building
Telephone: 3203
Email: zalakpatel.ec@indusuni.ac.in
Consultation times: 3:30 to 4:15 PM

Students will be contacted throughout the Session via Mail with important information relating to this Course.

Course Objectives

1. Basic concepts of modulation techniques including amplitude modulation frequency modulation (FM) and phase modulation (PM) that are widely used in analogue communication systems.
2. Basic concepts of a digital communication system including sampling theorem, pulse code modulation (PCM) and principles of digital data transmission, and basic techniques.
3. To study the concept of cellular system design.
4. To understand mobile technologies like GSM and CDMA.
5. To learn the basic elements of optical fiber transmission link, fiberglass modes, configurations and structures
6. To learn various optical sources, LED/LASER structures, receivers (PIN, APD), and noise performance
7. To provide understanding of different concepts used in a satellite communication system.

Course Outcomes (CO)

1. Use of different modulation and demodulation techniques used in analog & Digital communication.
2. Apply the sampling theorem to digitize the analog signal and recover original signal without any distortion.
3. Understand evolution of mobile communication generations 2G, 2.5G, and 3G with their characteristics and limitations.
4. Understand emerging technologies required for fourth generation mobile system such as SDR, MIMO etc.
5. Apply the fundamental principles of optics and light wave to design optical fiber communication systems.
6. Understands the basics of satellite communication and its different applications

Course Outline

(Key in topics to be dealt)

UNIT-I

Principles of modern communication system **[7 hours]**

Introduction, Communication Process, Channel Effect, Signal to noise ration & capacity, Amplitude modulation, Angle modulation, Sampling theorem, Pulse code modulation, Digital modulation techniques

UNIT-II

Wireless communication system **[8 hours]**

Introduction to Wireless Communication System-Evolution of mobile communications, the Cellular Concept System Design Fundamentals-Cellular system, Hexagonal geometry cell and concept of frequency reuse, Channel Assignment Strategies Distance to frequency reuse ratio, Channel & co-channel interference reduction factor, S/I ratio consideration and calculation for Minimum Co-channel and adjacent interference, Handoff Strategies, Umbrella Cell Concept, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular System-cell splitting, Cell sectorization, Repeaters, Micro cell zone concept, GSM,CDMA,OFDM & MIMO.

UNIT-III

Optical communication **[7hours]**

Evolution of Light wave systems, System components, Optical fibers – Step Index & Graded index -Mode theory, Numerical Aperture Fiber Losses, Optical transducer (LED,LASER,PIN and APD),FSO – Introduction ,Block diagram, Application Advantages & Limitation, Comparison of FSO with Fiber optics & other technologies.

UNIT-IV

Satellite Communication **[8 hours]**

Introduction to Satellite Communication,- Benefits of Satellite Communication, Types of Satellites, Satellite Services, satellite frequency bands, Satellite Orbits and Orbital Parameters- Types of orbits,Kepler's Law, Orbital elements ,Satellite orbits, Satellite Location from an Earth Station, Modern Developments and Future Trends- Micro- and Nanosatellites, Satellite Laser Communication, Software-defined Radio Technology.

Method of delivery

(Face to face lectures, self study material, Active Learning Techniques)

Study time

(5 hours per week including class attendance)

CO-PO Mapping (PO: Program Outcomes)

PO / CO	PO											
	1	2	3	4	5	6	7	8	9	10	11	12
1	√					√	√	√	√			
2	√					√	√	√				√
3		√		√							√	
4		√		√							√	
5			√		√				√	√		
6			√		√					√		√

Blooms Taxonomy and Knowledge retention(For reference)

(Blooms taxonomy has been given for reference)

Figure 1: Blooms Taxonomy

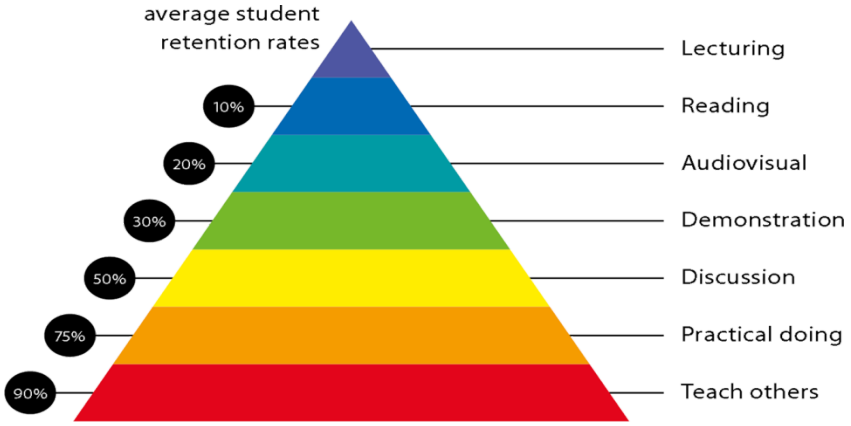

Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of _____Graduate Capabilities
Informed Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas.	**1 Professional knowledge, grounding & awareness**
Independent learners Engage with new ideas and ways of thinking and critically analyze issues. Seek to extend knowledge through ongoing research, enquiry and reflection. Find and evaluate information, using a variety of sources and technologies. Acknowledge the work and ideas of others.	**2 Information literacy, gathering & processing**

Problem solvers Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards.	**4 Problem solving skills**
Effective communicators Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in different settings. Recognize how culture can shape communication.	**5 Written communication** **6 Oral communication** **7 Teamwork**
Responsible Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.	**10 Sustainability, societal & environmental impact**

Lecture times

Lecture	Tuesday	8.30 – 9.25 am	Room LH 22
Lecture	Thursday	1.00 – 1.55 pm	Room LH 22
Lecture	Friday	1.55 -- 2.50 pm	Room LH 22

Attendance Requirements

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the Course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for mid and end semester examinations.

Details of referencing system to be used in written work

Text books

1. Modern Digital and Analog Communication Systems by B.P.Lathi 4th edition , Oxford

Additional Materials

Reference Books

1. "Fundamentals of Communication Systems – John G. Proakis and Masoud Salehi" Tata McGraw-Hill Publications
2. Dennis Roddy & John Coolen – Electronic Communication (IV Ed.), Prentice Hall of India.

Web Resources

1. https://nptel.ac.in/courses/117/105/117105144/
2. https://www.tutorialspoint.com/fundamentals_of_science_and_technology/communication_technology.

ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:

Example:

Quiz 1	10% (week 4)	Objective (1-3)
Class Test	10% (week 6)	Objective (1-4)
Seminar	10% (week 8)	Objective (1-4)
Mid semester	30% (due week 10)	Objectives (2-5)
Final exam (*closed book*)	40%	Objectives (1-5)

SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in mid semester or end semester will be considered for supplementary assessment in the respective components (i.e mid semester or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (mid semester or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of -% of the maximum mark per calendar day

Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

Retention of Written Work

Written assessment work will be retained by the Course coordinator/lecturer for two weeks after marking to be collected by the students.

University and Faculty Policies

Students should make themselves aware of the University and/or Faculty Policies regarding plagiarism, special consideration, supplementary examinations and other educational issues and student matters.

Plagiarism - Plagiarism is not acceptable and may result in the imposition of severe penalties. Plagiarism is the use of another person's work, or idea, as if it is his or her own - if you have any doubts at all on what constitutes plagiarism, please consult your Course coordinator or lecturer. Plagiarism will be penalized severely.

Do not copy the work of other students.
Do not share your work with other students (except where required for a group activity or assessment)

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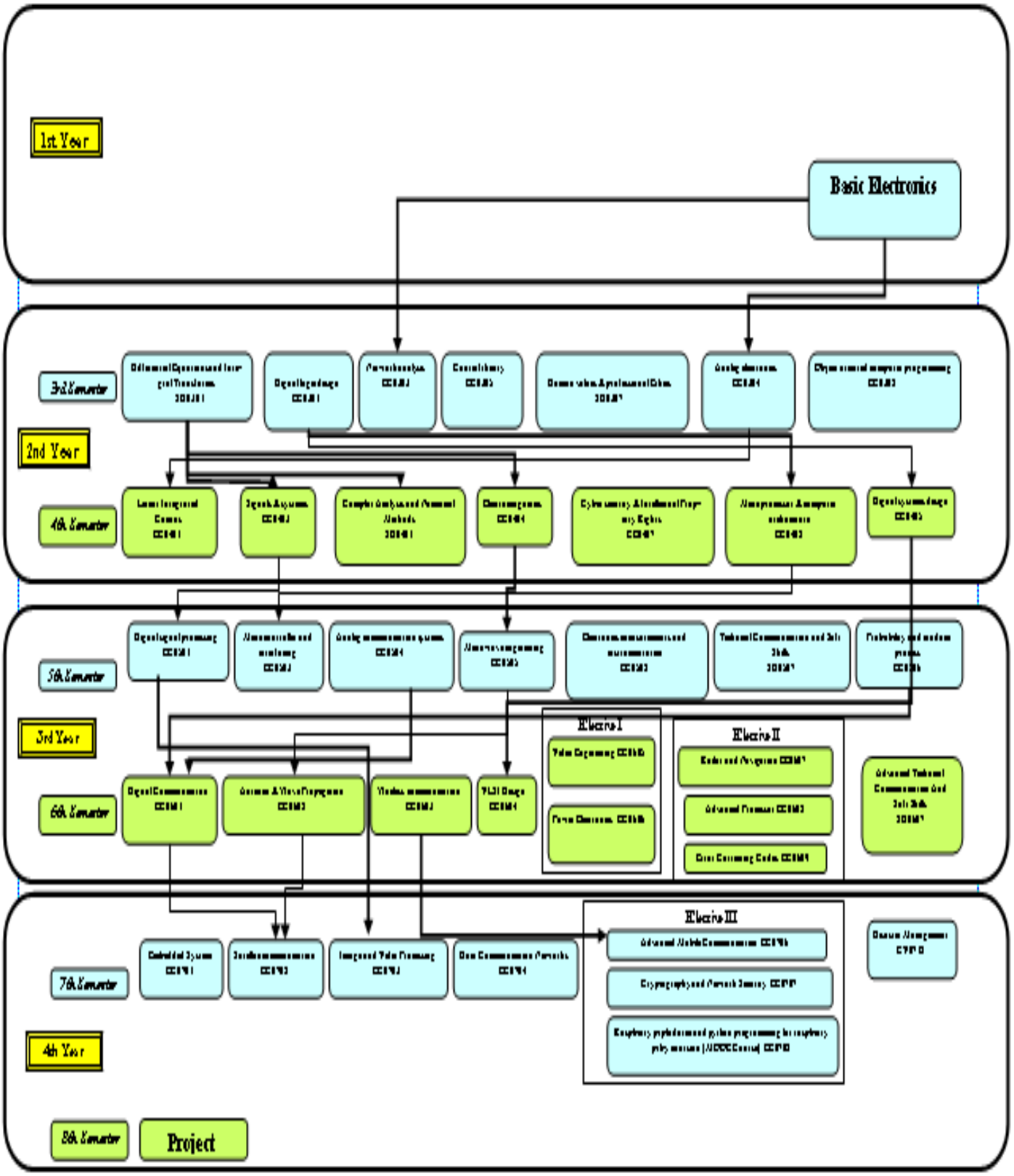
Course schedule (Modern Communication Systems)

(Mention quiz, assignment submission, breaks etc as well in the table under the Teaching Learning Activity Column)

	Week #	Topic & contents	CO Addressed	Teaching Learning Activity (TLA)
	Weeks 1	Communication Process, Channel Effect, Signal to noise ration & capacity	1,2	BB, PPT
	Weeks 2	Amplitude modulation, Angle modulation, Sampling theorem	1,2	BB, PPT
	Week 3	Pulse code modulation, Digital modulation techniques	1,2	BB, PPT
	Week 4	Introduction to Wireless Communication System-Evolution of mobile communications, The Cellular Concept System Design Fundamentals-Cellular system, Hexagonal geometry cell and concept of frequency reuse,	3,4	BB, PPT
	Week 5	Channel Assignment Strategies, Channel & co-channel interference reduction factor, S/I ratio consideration and calculation for minimum Co-channel and adjacent interference, Handoff Strategies	3,4	BB, PPT
	Week 6	Umbrella Cell Concept, Trunking and Grade of Service, Improving Coverage & Capacity in Cellular System-cell splitting, Cell sectorization, Repeaters, Micro cell zone concept	3,4	BB, PPT
	Week 7	GSM,CDMA,OFDM & MIMO	3,4	BB, PPT
	Week 8	Evolution of Light wave systems, System components, Optical fibers – Step Index & Graded index -Mode theory, Numerical Aperture Fiber Losses	5	PPT
	Week 9	Optical transducer (LED,LASER,PIN and APD),FSO – Introduction ,Block diagram, Application Advantages &	5	BB, PPT

		Limitation, Comparison of FSO with Fiber optics & other technologies		
	Week 10	Ground wave propagation, terrain and earth curvature effects, tropospheric propagation, fading, diffraction and scattering, Space wave propagation.	5	BB, PPT
	Week 11	Introduction to Satellite Communication,- Benefits of Satellite Communication, Types of Satellites, Satellite Services, satellite frequency bands	6	BB, PPT
	Week 12	Satellite Orbits and Orbital Parameters- Types of orbits, Kepler's Law, Orbital elements ,Satellite orbits	6	BB, PPT
	Week 13	Satellite Location from an Earth Station, Modern Developments and Future Trends- Micro- and Nanosatellites	6	BB, PPT
	Week 14	Satellite Laser Communication, Software-defined Radio Technology	6	BB, PPT
	Week 15	CIE evaluation-seminar presentations by students	1-6	PPT

PROGRAM MAP FOR B.Tech. (ELECTRONICS & COMMUNICATION ENGINEERING)



Name of Institute: Indus Institute of Technology and Engineering
Name of Faculty: Prof. Miloni Ganatra

Course code: EC0419
Course name: Digital System Design using HDL
Pre-requisites: Digital Logic Design
Credit points: 03
Offered Semester: 4th

Course Coordinator (weeks 15)
Full Name: Miloni Ganatra
Department with sitting location: 2nd Floor, EEE lab 2 , Bhanwar Building
Telephone: 9974592124
Email: miloniganatra.ee@indusuni.ac.in
Consultation times: Monday,Tuesday 3:45 to 4:15pm ,All working Saturdays

Course Lecturer (weeks 15)
Full Name: Miloni Ganatra
Department with siting location: 2nd Floor, EEE lab 2 , Bhanwar Building
Telephone: 9974592124
Email: miloniganatra.ee@indusuni.ac.in
Consultation times: Monday,Tuesday 3:45 to 4:15pm,All working Saturdays

Students will be contacted throughout the Session via Mail with important information relating to this Course.

Course Objectives

By participating in and understanding all facets of this Course a student will:

1) To familiarize the students with the conventions of the Verilog HDL programming,
2) To familiarize the students with algorithmic levels of abstraction for modeling of digital hardware systems.
3) To familiarize the students with the concept of test-benches to create testing behavioral environments for simulation based verification.
4) This course aims to provide students with the understanding of the different technologies related to HDLs, construct, compile and execute Verilog HDL programs using provided software tools

Course Outcomes (CO)

After completion this course the student will be able to

1) To understand the constructs and conventions of the Verilog HDL programming.

2) To understand the structural, register-transfer level (RTL), and algorithmic levels of abstraction for modelling digital hardware systems.
3) To design and modeling of combinational and sequential digital systems
4) To apply the concept of test-benches to create testing behavioural environments for simulation based verification.
5) To learn architecture of various reconfigurable devices.

Course Outline

UNIT-I

[12 hours]

Introduction to Verilog HDL: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification, System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools

Verilog Language Concept:
Code format, Logic Value system , Wires & variables ,Modules ,Module Port ,Names ,Numbers ,Arrays ,Verilog Operators & data Types ,Array Indexing

UNIT-II

[12 hours]

Gate Level Modeling:
Introduction, Gate level Primitive, Module Structure, Instances of Primitives, Gate Delays, Designing Using Primitives.

Modeling at Dataflow Level:
Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators.

UNIT-III

[12hours]

Behavioral Modeling:
Structured procedures, initial and always, blocking and non blocking statements, delay control, generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.

Functions, tasks, and user defined primitives: Introduction, Function, Tasks, User-Defined Primitives (UDP)

Component Test & Verification:
Test Bench - Combinational Circuits Testing, Sequential Circuit Testing, Design Verification, Assertion Verification

UNIT-IV

[12hours]

Reconfigurable Device Architectures:

Classification of FPGA, Basic architecture of CPLD and FPGA, Xilinx's CPLD and FPGA architecture.

Method of delivery

(Face to face lectures,PPT, **Chalkboard)**

Study time

(9 hours per week including class attendance)

CO-PO Mapping (PO: Program Outcomes)

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	1	1	-	3	2	-	-	1	-	-	-
CO2	3	3	3	1	3	1	-	-	-	-	-	-
CO3	1	2	3	1	3	2	-	-	-	-	-	-
CO4	1	1	3	2	2	-	-	-	-	-	-	-
CO5	1	2	1	3					1			

Blooms Taxonomy and Knowledge retention (For reference)

(Blooms taxonomy has been given for reference)

Figure 1: Blooms Taxonomy

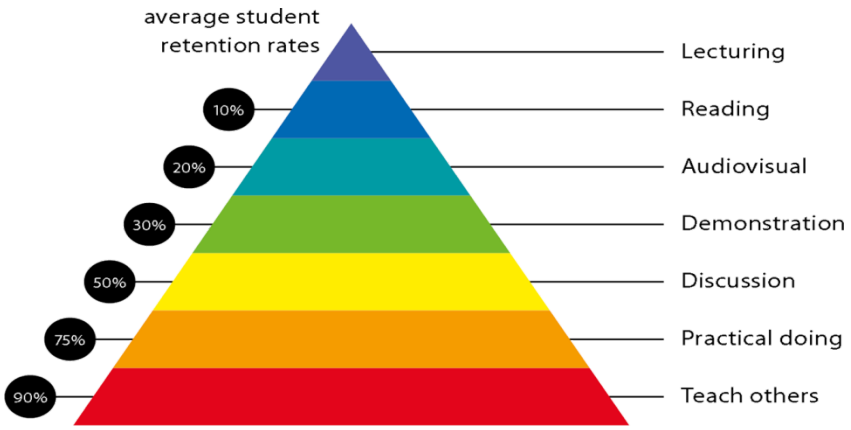


Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of __Electrical Graduate Capabilities
Informed Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas.	**1 Professional knowledge, grounding & awareness**
Independent learners Engage with new ideas and ways of thinking and critically analyze issues. Seek to extend knowledge through ongoing research, enquiry and reflection. Find and evaluate information, using a variety of sources and technologies. Acknowledge the work and ideas of others.	**2 Information literacy, gathering & processing**
Problem solvers Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards.	**4 Problem solving skills**
Effective communicators Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in	**5 Written communication** **6 Oral communication** **7 Teamwork**

different settings. Recognize how culture can shape communication.	
Responsible Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.	**10 Sustainability, societal & environmental impact**

Practical work:

List of Lab Experiment:

A. Introduction to Basic Syntax of Verilog and Gate level Modelling through implementation of half adder at gate level and its simulation & synthesize using Xilinx ISE tools.

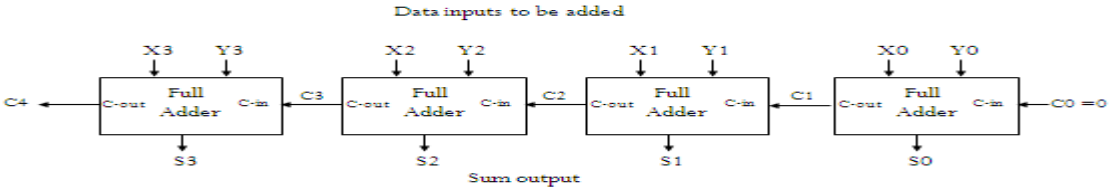
B. Design following Combinational & Sequential Circuits using Data Flow/Behavioural Verilog Coding, Consolidation of the concepts of Test Bench module & simulate and synthesize using Xilinx ISE tools.

1. Half Adder,Full Adder ,Half Subtractor & Full Subtractor
2. 4 bit magnitude Comparator
3. 4:1 ,8:1 Multiplexer
4. 3-8 ,4-16 decoder
5. 8-3 ,16-4 Encoder
6. BCD to seven Segment Decoder in VHDL (common anode & common Cathode)
7. JK,RS,T,D Flip flop (+ve and –ve edge triggering) & JK,RS,T,D Latch using if & Case Statement
8. 1-4 Demux with enable input.
9. Design of 4 Bit Binary to BCD Converter using sequential statement.
10. Prepare a module to generate 2's,9's complement of a 4-bit number.
11. 8 bit odd/even parity checker/generator.
12. Implement Binary to Gray converter.
13. Implement BCD to XS-3 code converter
14. Implement binary to BCD code converter
15. Implement to GRAY to BINARY code converter using VHDL.
16. 4-bit Serial In Parallel Out (SIPO) Shift Register using variable

17. 4-bit Parallel In Parallel Out (PIPO) Shift Register using variable
18. Up Counter (Program for 4-bit binary counter using behavior description)
19. Down Counter (Program for 4-bit binary counter using behavior description)
20. Up/Down Counter (Program for 4-bit binary counter using behavior description)
21. Mod N Counter (Up, Down, Up/Down) Mod-3,5,6,7,9,11

C. Design following Combinational & Sequential Circuits using Data Flow/Behavioural Verilog Coding, Consolidation of the concepts of Test Bench module & simulate and synthesize using Xilinx ISE tools.

1. 4 bit Asynchronous counter using Structural Modeling (use D Flip Flop as a component) .
2. 4 bit Synchronous counter using Structural Modeling (use D Flip Flop as UDP) .
3. Mod 5 Counter (up,Down,Up/Down) (using T or J-K flip flop as UDP)
4. Full adder with structural style of coding. (Use half adder & OR gate as UDP)
5. 4 to 1 Mux Implementation (use 2 to 1 Mux as UDP)
6. program for 4-16 decoder using structural Modelling (use 3-8 decoder as UDP)
7. A master-slave D ,JK,RS,T Flip flop (use D ,JK,RS,T flip flop as UDP)
8. 4 bit parallel adder. (4-bit Ripple Carry Adder) using structural modeling (use full adder as UDP)



Lecture/tutorial times

Example:
Lecture
Monday- 1:30 PM-2:25 PM
Tuesday- 9:55 PM- 10:50 PM
Practical
Monday- 11-00 PM-12-50PM
Wednesday-11-00 PM-12-50PM

Attendance Requirements

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the Course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for mid and end semester examinations.

Details of referencing system to be used in written work

Text books

1) Zainalabdien Navabi, Verliog Digital System Design,TMH, 2nd Edition.
2) Verilog HDL - Samir Palnitkar, 2nd Edition, Pearson Education, 2009.

Additional Materials

Reference books

1) Fundamentals of Digital Logic with Verilog Design - Stephen Brown,Zvonkoc Vranesic, TMH, 2nd Edition.
2) Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.
3) T.R. Padmanabhan, B Bala Tripura Sundari, Design Through Verilog HDL, Wiley 2009.
4) Advanced Digital Design with Verilog HDL - Michel D. Ciletti, PHI,2009.

Web Resource

1) Digital system Design course on NPTEL (http://nptel.ac.in/courses/117108040) 3.
2) Online free course on Verilog-HDL (http://vol.verilog.com/) 4.
3) Online free course on Verilog-HDL by ALTERA (https://www.altera.com/support/training/course/ohdl1120.html) 5. EDAPlayground - Online
4) Verilog/VHDL complier (https://www.edaplayground.com/)

ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:

Theory:
Class Test 1 (20 Marks)
Class Test 2 (20 Marks)
Seminar Presentation (20 Marks)
ESE (40 Marks)

S

Practical:
Mini Project (20 Marks)
Practical Performance + Lab manual (40 Marks)

SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in mid semester or end semester will be considered for supplementary assessment in the respective components (i.e mid semester or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (mid semester or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of -% of the maximum mark per calendar day

Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

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Do not copy the work of other students.
Do not share your work with other students (except where required for a group activity or assessment)

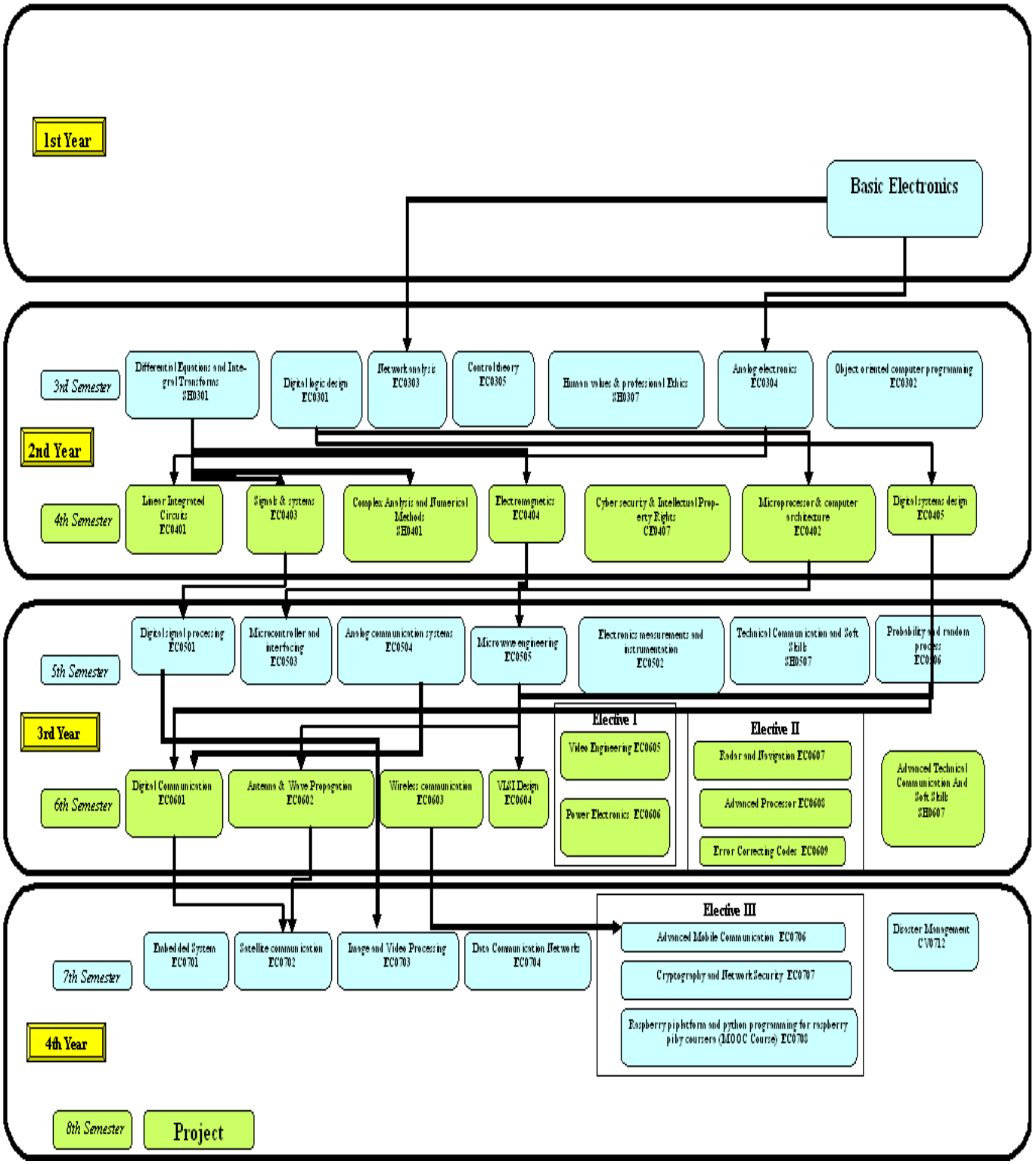
.

Course schedule (subject to change)

	Week #	Topic & contents	CO Addressed	Teaching Learning Activity (TLA)
	Weeks 1	**Introduction to Verilog HDL:** Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Function Verification,	1,2	BB,PPT
	Weeks 2	**Introduction to Verilog HDL:** System Tasks, Programming Language Interface, Module, Simulation and Synthesis Tools	1,2	BB,PPT
	Week 3	**Verilog Language Concept:** Code format, Logic Value system , Wires & variables	1,2	BB,PPT
	Week 4	**Verilog Language Concept:** Modules ,Module Port ,Names ,Numbers, Arrays ,Verilog Operators & data Types ,Array Indexing	1,2	BB,PPT
	Week 5	**Gate Level Modeling:** Introduction, Gate level Primitive, Module Structure	2,3	BB,PPT
	Week 6	**Gate Level Modeling:** Instances of Primitives, Gate Delays, Designing Using Primitives	2,3	BB,PPT
	Week 7	**Modeling at Dataflow Level:** Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators.	2,3	BB,PPT
	Week 8	**Behavioral Modeling:** Structured procedures, initial and always, blocking and non blocking statements, delay control	2,3	BB,PPT
	Week 9	**Behavioral Modeling:** generate statement, event control, conditional statements, multiway branching, loops, sequential and parallel blocks.	2,3	BB,PPT

	Week 10	**Functions, tasks, and user defined primitives:** Introduction, Function, Tasks, User- Defined Primitives (UDP)	3,4	BB,PPT
	Week 11	**Component Test & Verification:** Test Bench - Combinational Circuits Testing	3,4	BB,PPT
	Week 12	**Component Test & Verification:** Test Bench - Sequential Circuit Testing	3,4	BB,PPT
	Week 13	**Component Test & Verification:** Design Verification, Assertion Verification	3,4	BB,PPT
	Week 14	**Reconfigurable Device Architectures:** Classification of FPGA, Basic architecture of CPLD and FPGA	5	BB,PPT
	Week 15	**Reconfigurable Device Architectures:** Xilinx's CPLD and FPGA architecture.	5	BB,PPT

Program map for B.Tech (Electronics & Communication Engineering)



Name of Institute: Institute of Technology and Engineering
Name of Faculty: Dr. Vrushank Shah

Course code: EC0421
Course name: Signals and Systems
Pre-requisites: Mathematics
Credit points: 03
Offered Semester: IV

Course coordinator (weeks 1 - 14)
Full name: Dr. Vrushank Shah
Department with siting location: 3rd floor, Faculty Room, Bhanwar Building
Telephone: 9898331721, Intercom:3325
Email:ec.hod@indusuni.ac.in
Consultation times: 4:00 PM to 5:00 PM

Course lecturer (weeks 1 - 14)
Full name: Dr. Vrushank Shah
Department with siting location: 3rd floor, Faculty Room, Bhanwar Building
Telephone: 9898331721, Intercom:3325
Email:ec.hod@indusuni.ac.in
Consultation times: 4:00 PM to 5:00 PM

Students will be contacted throughout the session via mail with important information relating to this course.

Course Objectives

By participating in and understanding all facets of this course a student will:

1. Coverage of continuous and discrete-time signals and systems, their properties and representations and methods those are necessary for the analysis of continuous and discrete-time signals and systems.
2. Knowledge of time-domain representation and analysis concepts as they relate to difference equations, impulse response and convolution, etc
3. Concepts of the sampling process
4. Knowledge of frequency-domain representation and analysis concepts using Fourier analysis tools, Z-transform, Laplace Transform.

Course Outcomes (CO)

1. Students will be able to represent & classify signals, Systems & identify LTI systems
2. Students will be able to derive Fourier series for continuous & Discrete time signals
3. Students will be able to find Fourier transform for different signals
4. Students will be able to analyze systems by performing Convolution
5. Students will be able to analyze DT systems using Z-transforms & Laplace Transform.

Course Outline

UNIT-I

[12 hours]

INTRODUCTION

- Definitions and concepts of different types of signals;
- Continuous-time and discrete-time signals;
- Mathematical operation on Discrete time signals
- Systems: Continuous-time and Discrete-time systems and basic system properties.
- Sampling of Continuous time signals
- Response of LTI Discrete time system in time domain.
- Linear convolution
- Impulse response
- Circular Convolution
- Correlation
- Relation between convolution and correlation

UNIT-II

FOURIER SERIES **[15 hours]**

- Representation of Fourier series,
- Continuous time periodic signals,
- Fourier series for discrete time signals
- Properties of Fourier series,
- Gibbs phenomenon
- Dirichlet's conditions

FOURIER TRANSFORMS

- Deriving Fourier transform from Fourier series,
- Properties of Fourier transforms,
- Introduction to Hilbert Transform
- Analysis of LTI discrete time system using discrete time Fourier transform
- Aliasing in frequency spectrum due to sampling

UNIT-III

LAPLACE TRANSFORMS **[15 hours]**

- Review of Laplace transforms, Partial fraction expansion,
- Inverse Laplace transform,
- Concept of region of convergence (ROC) for Laplace transforms, constraints on ROC for various classes of signals,
- Properties of L.T's relation between L.T's, and F.T. of a signal.
- Laplace transform of certain signals using waveform synthesis
- Analysis of LTI continuous time system using Laplace Transform

UNIT-IV

Z–TRANSFORMS **[12 hours]**

- Concept of Z- Transform of a discrete sequence.
- Distinction between Laplace, Fourier and Z transforms.

- Region of convergence in Z-Transform, constraints on ROC for various classes of signals, Inverse Z-transform, properties of Z-transforms.
- Analysis of LTI continuous time system using Z-transform Transform

Method of delivery

Face to face lectures, self-study material, Active Learning Techniques, PowerPoint Presentations, Assignments

Study time

Lecture hours: 3 hours

CO-PO Mapping (PO: Program Outcomes)

CO \ PO	PO 1	2	3	4	5	6	7	8	9	10	11	12
1	√				√	√	√	√				
2	√				√	√	√	√				
3		√			√					√		
4		√								√		
5	√		√									

Blooms Taxonomy and Knowledge retention (For reference)

(Blooms taxonomy has been given for reference)

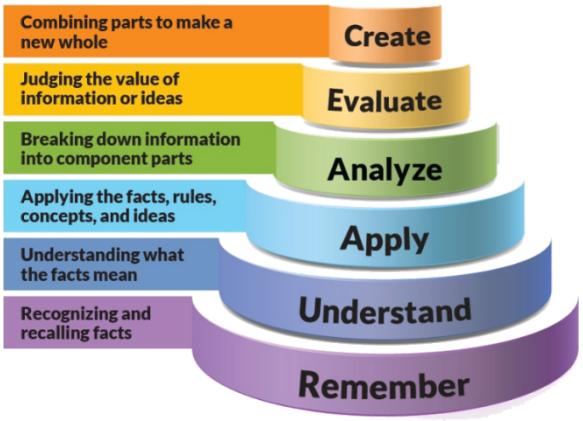


Figure 1: Blooms Taxonomy

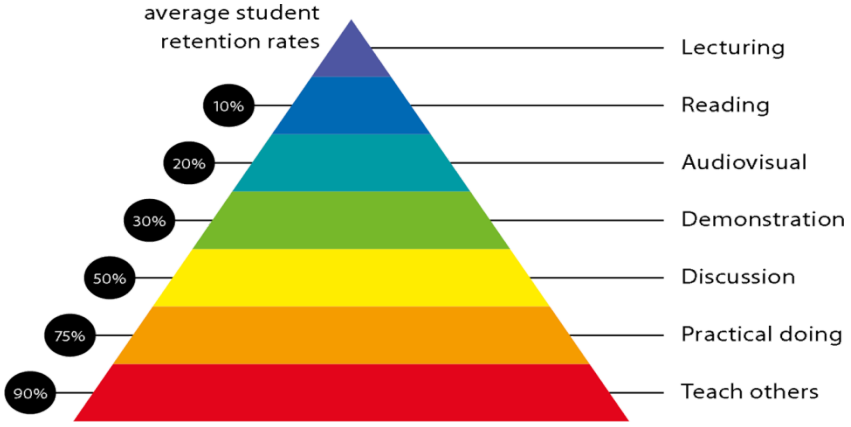


Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of Electronics and Communication Graduate Capabilities
Informed Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas.	**1 Professional knowledge, grounding & awareness**
Independent learners Engage with new ideas and ways of thinking and critically analyze issues. Seek to extend knowledge through ongoing research, enquiry and reflection. Find and evaluate information, using a variety of sources and technologies. Acknowledge the work and ideas of others.	**2 Information literacy, gathering & processing**
Problem solvers Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards.	**4 Problem solving skills**
Effective communicators Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in different settings. Recognize how culture can shape communication.	**5 Written communication** **6 Oral communication** **7 Teamwork**

Responsible Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.	**10 Sustainability, societal & environmental impact**

Practical work:

(Mention what practical work this Course involves)

Not Applicable

Lecture/tutorial times

(Give lecture times in the format below)

Under Preparation

Attendance Requirements

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for semester examinations.

Details of referencing system to be used in written work

Text books

1. Alan V. Oppenheim, A. S. Willsky "Signals and Systems", PHI
2. A Nagoor Kani ,"Signals & Systems ",Mc Graw Hill..

Additional Materials

1. Ramakrishna Rao, P, "Signals and Systems" Tata McGraw Hill, 2008.
2. Simon Haykin and Barry Van Veen, "Signals & Systems", John Wiley and Sons Inc., New Delhi, 2008.

ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:

EC

Example: **Quiz 1** 10% (week 4) Objective (1-3) **Quiz II** 10% (week 8) Objective (1-4) **Simulation Exercises 20% (week 1-14) Objective(1-4)** **Class Test** 20% (week 7) Objectives (2-4) **Final exam** (*closed book*) 40% Objectives (1-4)

SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in internal component or less than 40% in the end semester will be considered for supplementary assessment in the respective components (i.e internal component or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (internal component or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of -% of the maximum mark per calendar day

Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

Retention of Written Work

Written assessment work will be retained by the Course coordinator/lecturer for two weeks after marking to be collected by the students.

University and Faculty Policies

Students should make themselves aware of the University and/or Faculty Policies regarding plagiarism, special consideration, supplementary examinations and other educational issues and student matters.

Plagiarism - Plagiarism is not acceptable and may result in the imposition of severe penalties. Plagiarism is the use of another person's work, or idea, as if it is his or her own - if you have any doubts at all on what constitutes plagiarism, please consult your Course coordinator or lecturer. Plagiarism will be penalized severely.

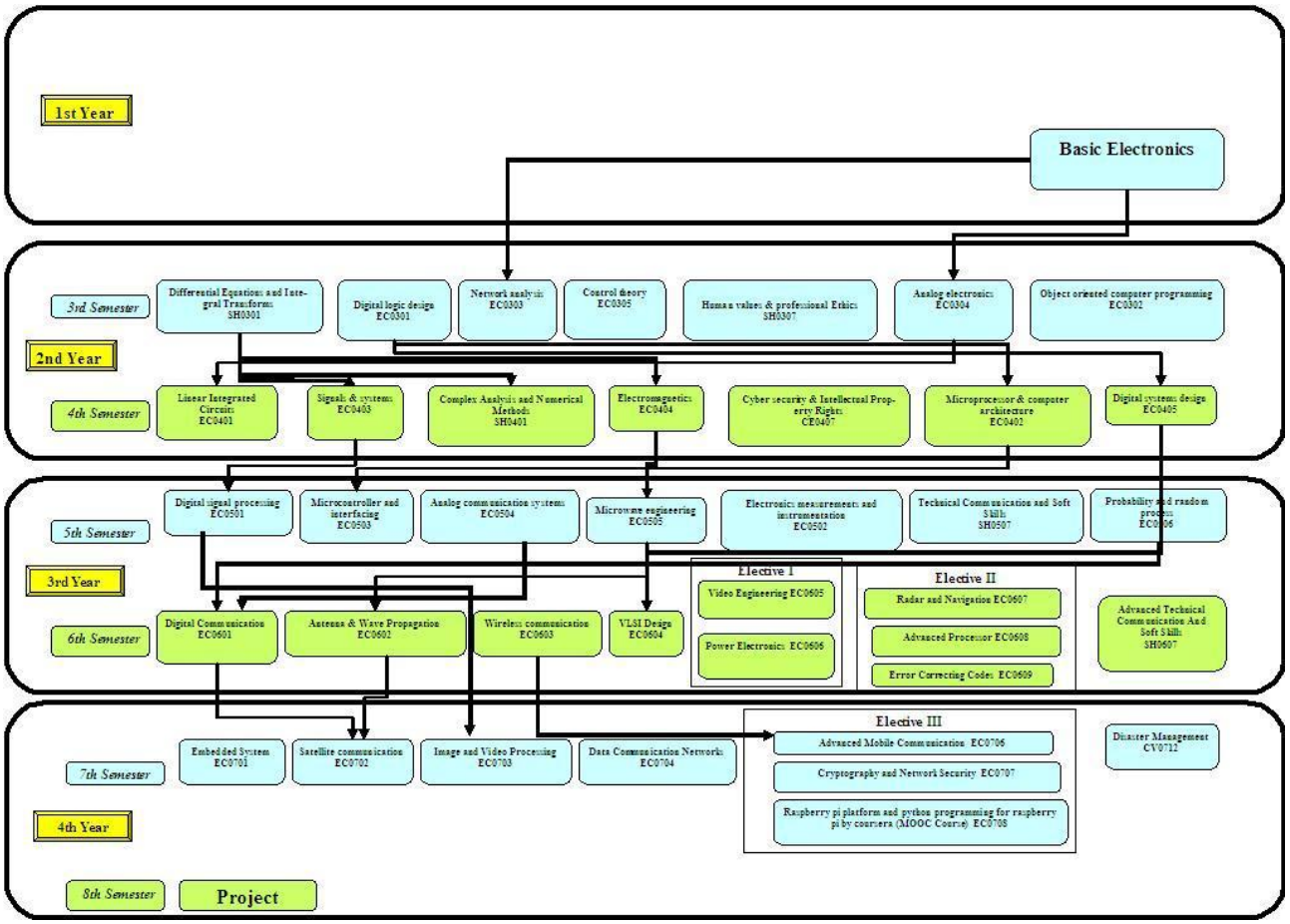
Do not copy the work of other students.
Do not share your work with other students (except where required for a group activity or assessment).

Course schedule (subject to change)

(Mention quiz, assignment submission, breaks etc as well in the table under the Teaching Learning Activity Column)

	Week #	Topic & contents	CO Addressed	Teaching Learning Activity (TLA)
	Weeks 1	Definitions and concepts of different types of signals; Continuous-time and discrete-time signals; Mathematical operation on Discrete time signals, Systems: Continuous-time and Discrete-time systems and basic system properties., Sampling of Continuous time signals , Response of LTI Discrete time system in time domain.	1-2	BB,Chalk,PPT
	Weeks 2	Linear convolution, Impulse response, Circular Convolution , Correlation, Relation between convolution and correlation	1-2	BB,Chalk,PPT
	Week 3	Representation of Fourier series, Continuous time periodic signals, Fourier series for discrete time signals	*1-2*	BB,Chalk,PPT
	Week 4	Properties of Fourier series, Gibbs phenomenon, Dirichlet's conditions,	1-2-3	BB,Chalk,PPT
	Week 5	Deriving Fourier transform from Fourier series, ,	2-3	BB,Chalk,PPT
	Week 6	Properties of L.T's relation between L.T's, and F.T. of a signal. Laplace transform of certain signals using waveform synthesis. Analysis of LTI continuous time system using Laplace Transform	*2-3*	BB,Chalk,PPT
	Week 7	Properties of Fourier transforms, Introduction to Hilbert Transform	2-3	BB,Chalk,PPT
	Week 8	Analysis of LTI discrete time system using discrete time Fourier transform. Aliasing in frequency spectrum due to sampling	2-3	BB,Chalk,PPT
	Week 9	Review of Laplace transforms, Partial fraction expansion, Inverse Laplace transform,	*4*	BB,Chalk,PPT

	Week 10	Concept of region of convergence (ROC) for Laplace transforms, constraints on ROC for various classes of signals, Properties of L.T's relation between L.T's, and F.T. of a signal.	4	BB,Chalk,PPT
	Week 11	Laplace transform of certain signals using waveform synthesis. Analysis of LTI continuous time system using Laplace Transform	4	BB,Chalk,PPT
	Week 12	Concept of Z- Transform of a discrete sequence. Distinction between Laplace, Fourier and Z transforms	4-5	BB,Chalk,PPT
	Week 13	Region of convergence in Z-Transform, constraints on ROC for various classes of signals, Inverse Z-transform, properties of Z-transforms	4-5	BB,Chalk,PPT
	Week 14	Analysis of LTI continuous time system using Z-transform Transform	4-5	BB,Chalk,PPT


1st Year
Basic Electronics
3rd Semester
Differential Equations and Integral Transforms SH0301
Digital logic design EC0301
Network analysis EC0303
Control theory EC0305
Human values & professional Ethics SH0307
Analog electronics EC0304
Object oriented computer programming EC0302
2nd Year
4th Semester
Linear Integrated Circuits EC0401
Signals & systems EC0403
Complex Analysis and Numerical Methods SH0401
Electromagnetics EC0404
Cyber security & Intellectual Property Rights CE0407
Microprocessor & computer architecture EC0402
Digital systems design EC0405
5th Semester
Digital signal processing EC0501
Microcontroller and interfacing EC0503
Analog communication systems EC0504
Microwave engineering EC0505
Electronics measurements and instrumentation EC0502
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Probability and random process EC0506
3rd Year
Elective I
Video Engineering EC0605
Power Electronics EC0606
Elective II
Radar and Navigation EC0607
Advanced Processor EC0608
Error Correcting Codes EC0609
6th Semester
Digital Communication EC0601
Antenna & Wave Propagation EC0602
Wireless communication EC0603
VLSI Design EC0604
Advanced Technical Communication And Soft Skills SH0507
Elective III
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Cryptography and Network Security EC0707
Raspberry pi platform and python programming for raspberry pi by coursera (MOOC Course) EC0708
Disaster Management CV0712
7th Semester
Embedded System EC0701
Satellite communication EC0702
Image and Video Processing EC0703
Data Communication Network EC0704
4th Year
8th Semester
Project

Name of Institute: Institute of Technology and Engineering
Name of Faculty: Dr. Vrushank Shah

Course code: EC0421
Course name: Signals and Systems
Pre-requisites: Mathematics
Credit points: 03
Offered Semester: IV

Course coordinator (weeks 1 - 14)
Full name: Dr. Vrushank Shah
Department with siting location: 3rd floor, Faculty Room, Bhanwar Building
Telephone: 9898331721, Intercom:3325
Email:ec.hod@indusuni.ac.in
Consultation times: 4:00 PM to 5:00 PM

Course lecturer (weeks 1 - 14)
Full name: Dr. Vrushank Shah
Department with siting location: 3rd floor, Faculty Room, Bhanwar Building
Telephone: 9898331721, Intercom:3325
Email:ec.hod@indusuni.ac.in
Consultation times: 4:00 PM to 5:00 PM

Students will be contacted throughout the session via mail with important information relating to this course.

Course Objectives

By participating in and understanding all facets of this course a student will:

1. Coverage of continuous and discrete-time signals and systems, their properties and representations and methods those are necessary for the analysis of continuous and discrete-time signals and systems.
2. Knowledge of time-domain representation and analysis concepts as they relate to difference equations, impulse response and convolution, etc
3. Concepts of the sampling process
4. Knowledge of frequency-domain representation and analysis concepts using Fourier analysis tools, Z-transform, Laplace Transform.

Course Outcomes (CO)

1. Students will be able to represent & classify signals, Systems & identify LTI systems
2. Students will be able to derive Fourier series for continuous & Discrete time signals
3. Students will be able to find Fourier transform for different signals
4. Students will be able to analyze systems by performing Convolution
5. Students will be able to analyze DT systems using Z-transforms & Laplace Transform.

Course Outline

UNIT-I

[12 hours]

INTRODUCTION

- Definitions and concepts of different types of signals;
- Continuous-time and discrete-time signals;
- Mathematical operation on Discrete time signals
- Systems: Continuous-time and Discrete-time systems and basic system properties.
- Sampling of Continuous time signals
- Response of LTI Discrete time system in time domain.
- Linear convolution
- Impulse response
- Circular Convolution
- Correlation
- Relation between convolution and correlation

UNIT-II

FOURIER SERIES **[15 hours]**

- Representation of Fourier series,
- Continuous time periodic signals,
- Fourier series for discrete time signals
- Properties of Fourier series,
- Gibbs phenomenon
- Dirichlet's conditions

FOURIER TRANSFORMS

- Deriving Fourier transform from Fourier series,
- Properties of Fourier transforms,
- Introduction to Hilbert Transform
- Analysis of LTI discrete time system using discrete time Fourier transform
- Aliasing in frequency spectrum due to sampling

UNIT-III

LAPLACE TRANSFORMS **[15 hours]**

- Review of Laplace transforms, Partial fraction expansion,
- Inverse Laplace transform,
- Concept of region of convergence (ROC) for Laplace transforms, constraints on ROC for various classes of signals,
- Properties of L.T's relation between L.T's, and F.T. of a signal.
- Laplace transform of certain signals using waveform synthesis
- Analysis of LTI continuous time system using Laplace Transform

UNIT-IV

Z–TRANSFORMS **[12 hours]**

- Concept of Z- Transform of a discrete sequence.
- Distinction between Laplace, Fourier and Z transforms.

- Region of convergence in Z-Transform, constraints on ROC for various classes of signals, Inverse Z-transform, properties of Z-transforms.
- Analysis of LTI continuous time system using Z-transform Transform

Method of delivery

Face to face lectures, self-study material, Active Learning Techniques, PowerPoint Presentations, Assignments

Study time

Lecture hours: 3 hours

CO-PO Mapping (PO: Program Outcomes)

CO \ PO	PO 1	2	3	4	5	6	7	8	9	10	11	12
1	√				√	√	√	√				
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3		√			√					√		
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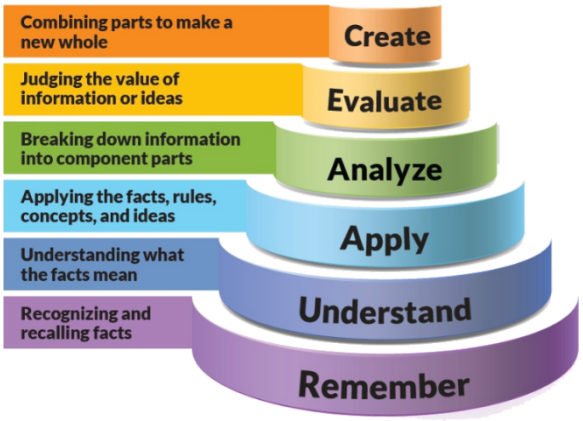
Blooms Taxonomy and Knowledge retention (For reference)

(Blooms taxonomy has been given for reference)



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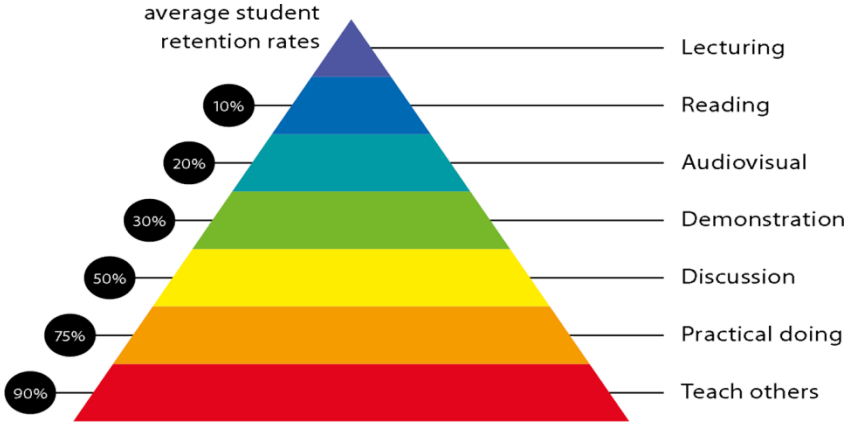

Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of Electronics and Communication Graduate Capabilities
Informed Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas.	**1 Professional knowledge, grounding & awareness**
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Practical work:

(Mention what practical work this Course involves)

Not Applicable

Lecture/tutorial times

(Give lecture times in the format below)

Under Preparation

Attendance Requirements

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Course schedule (subject to change)

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	Week 10	Concept of region of convergence (ROC) for Laplace transforms, constraints on ROC for various classes of signals, Properties of L.T's relation between L.T's, and F.T. of a signal.	4	BB,Chalk,PPT
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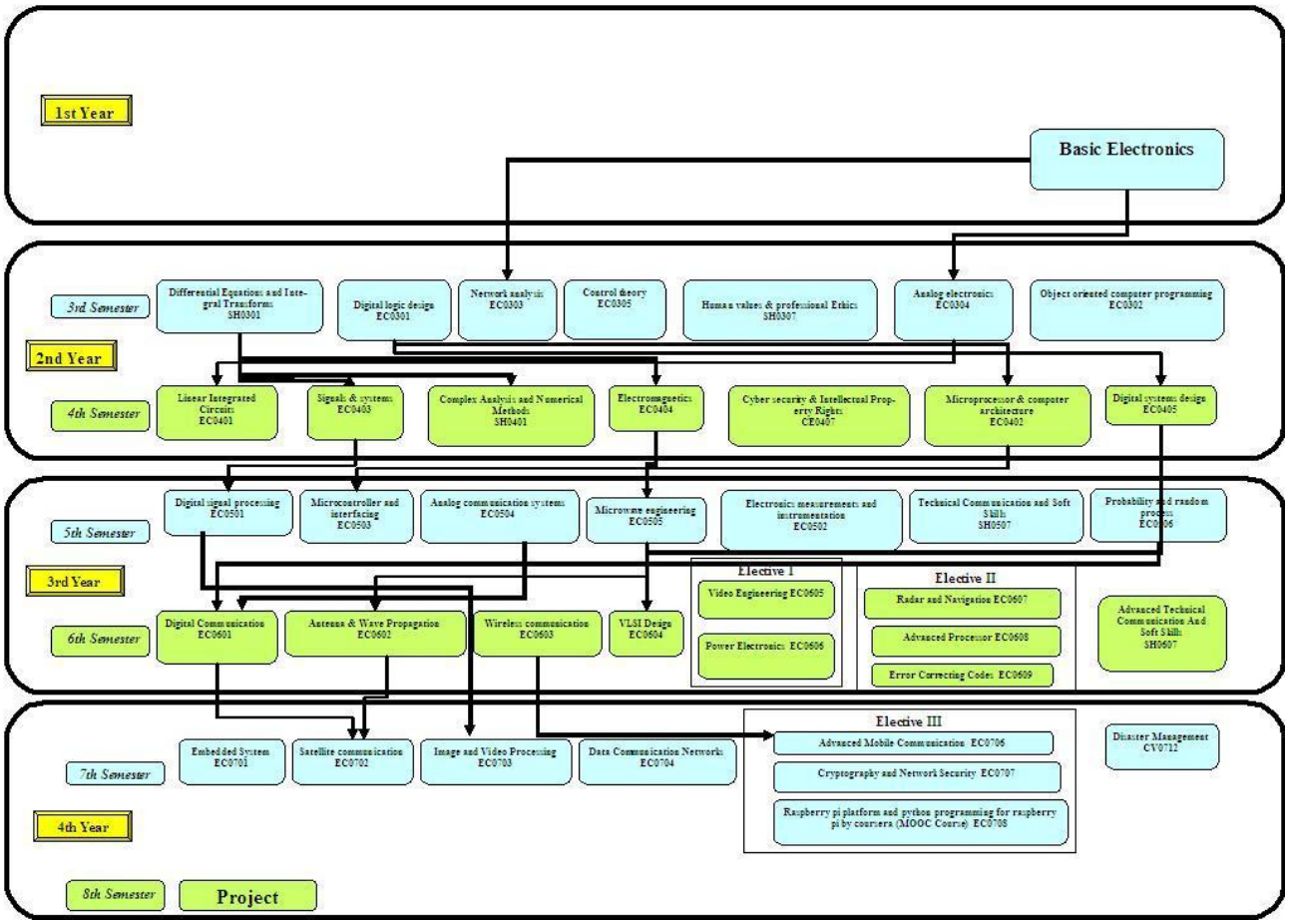
	Week 13	Region of convergence in Z-Transform, constraints on ROC for various classes of signals, Inverse Z-transform, properties of Z-transforms	4-5	BB,Chalk,PPT
	Week 14	Analysis of LTI continuous time system using Z-transform Transform	4-5	BB,Chalk,PPT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Control theory EC0305
Human values & professional Ethics SH0307
Analog electronics EC0304
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2nd Year
4th Semester
Linear Integrated Circuits EC0401
Signals & systems EC0403
Complex Analysis and Numerical Methods SH0401
Electromagnetics EC0404
Cyber security & Intellectual Property Rights CE0407
Microprocessor & computer architecture EC0402
Digital systems design EC0405
5th Semester
Digital signal processing EC0501
Microcontroller and interfacing EC0503
Analog communication systems EC0504
Microwave engineering EC0505
Electronics measurements and instrumentation EC0502
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Probability and random process EC0506
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Power Electronics EC0606
Elective II
Radar and Navigation EC0607
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Error Correcting Codes EC0609
6th Semester
Digital Communication EC0601
Antenna & Wave Propagation EC0602
Wireless communication EC0603
VLSI Design EC0604
Advanced Technical Communication And Soft Skills SH0507
Elective III
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Cryptography and Network Security EC0707
Raspberry pi platform and python programming for raspberry pi by coursera (MOOC Course) EC0708
Disaster Management CV0712
7th Semester
Embedded System EC0701
Satellite communication EC0702
Image and Video Processing EC0703
Data Communication Network EC0704
4th Year
8th Semester
Project

Name of Institute: Indus Institute of Technology and Engineering
Name of Faculty: Dr Minesh P Thaker

Course code: EC 0401
Course name: Linear Integrated Circuits
Pre-requisites: Basic Electronics
Credit points: 4
Offered Semester: IV the

Course Coordinator (weeks 01 – 16)
Full Name: Dr Minesh P Thaker
Department with sitting location:EC LAB 6
Telephone: 3201
Email: mineshthaker.ec@indusuni.ac.in
Consultation times:

Students will be contacted throughout the Session via **Google Classroom** with important information relating to this Course.

Course Objectives

By participating in and understanding all facets of this Course a student will:

1) **Study** the basic principles, configurations and practical limitations of op-amp.
2) **Analyse** , **design**, **construct** and **create** various linear and non-linear applications of op-amp
3) **Analyze** and **design** op-amp oscillators, single chip oscillators and frequency generators
4) **Analyze**, **design** and **explain** the characteristics and applications of active filters, including the switched capacitor filter
5) **Understand** ,**design construct** and **create** the most commonly used Power supplies(78xx,79xx,LM723 etc.) and Timer ICs(555)

Course Outcomes (CO)

CO1	To **explain** the op-amp's basic construction, characteristics, parameter limitations, various configurations and countless applications of op-amp.
CO2	To **compare** and **select** the various operational amplifier ICs using performance parameter given in the data sheets
CO3	To **analyze** basic op-amp circuits, particularly various linear and non-linear circuits, active filters, signal generators, and data converters
CO4	To **design** basic op-amp circuits, particularly various linear and non-linear circuits, active filters, signal generators, and data converters

CO5	To **apply** the concepts of op-amps and become proficient with computer skills (eg., Multisim) for the analysis and design of circuits
CO6	To **create** the analog circuit system for domestic applications

Course Outline

(Key in topics to be dealt)

UNIT I		
Chapter	**Titles**	**Hrs**
Chapter 1	Circuit Symbol, and terminals, basic Operational amplifier circuit, voltage follower Circuit, non inverting and inverting amplifier	3
Chapter 2	Operational Amplifier Parameter and Performances, Ideal and Practical Operational Amplifier, Input Output and Supply voltages, offset voltages and currents, Input and Output Impedances, Slew rate and frequency limitations	4
Chapter 3	Summing Amplifier, Difference Amplifier, Instrumentation Amplifier	5
UNIT II		
Chapter 7	Current to Voltage Converter, Basic Log and basic Anti Log Amplifier	6
Chapter 8	Voltage Level Detector, Schmitt Trigger Circuits, Comparator, Differentiator, Integrator.	5
UNIT III		
Chapter 9	Precision Half wave and Full wave Rectifier circuits	5
Chapter 10	Tri-angular Wave Generator, 555 Timer, Mono-stable A-stable Multi-vibrator Design and Analysis	6
UNIT IV		
Chapter 12	Active Filter Design calculations for First order and Second order low pass filters	5
Chapter 13	Fixed and Adjustable voltage regulators	3
Chapter 15	Analog to digital conversion basics and Digital to analog Convertion,	3

Method of delivery

(Face to face lectures, self study material, Active Learning Techniques)

Face to Face lectures via power point presentations and chalk-Blackboard

Study time

(How many hours per week including class attendance)

3 hours Theory

2 Hours Lab

CO-PO Mapping (PO: Program Outcomes)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO1 0	PO1 1	PO1 2
CO 1	3	3	3	3	3	-	2	1	1-	1	1	1
CO 2	3	2	3	1	3	-	-	-	-	-	-	-
CO 3	3	2	2	2	3	-	-	-	-	-	-	-
CO 4	3	2	1	-	-	-	-	-	-	-	-	1
CO 5	3	2	3	1	3	-	3	3	-	-	-	1
CO 6	3	3	1	1	3	-	3	3	-	-	-	1

Blooms Taxonomyand Knowledge retention(For reference)

(Blooms taxonomy has been given for reference)

Figure 1: Blooms Taxonomy

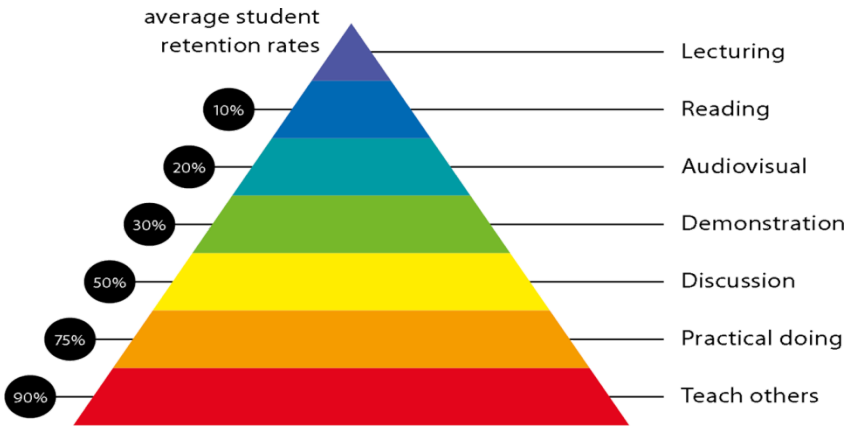

Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of EC_Graduate Capabilities
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Problem solvers Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards.	**4 Problem solving skills**
Effective communicators	**5 Written communication**
	6 Oral communication

Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in different settings. Recognize how culture can shape communication.	**7 Teamwork**
Responsible Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.	**10 Sustainability, societal & environmental impact**

Practical work:

(Mention what practical work this Course involves)

Lecture/tutorial times

(Give lecture times in the format below)

Example:

A

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the Course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for mid and end semester examinations.

Details of referencing system to be used in written work

Text books

T1	**Text Book** David A Bell, "Operational Amplifier and Linear IC's", Third Edition, Oxford University Press, ISBN 13: 9780195696134
R1	**Reference Books** Ramakant Gayakwad "Op-amps and Linear Integrated Circuits", 4/e, PHI publication, ISBN 13: 9788120320581
R2	Sergio Franco "Design with Operational Amplifiers and Analog Integrated Circuits", Tata Mcgraw-hill 2009 Edition, ISBN 13: 9780070217997

R3	D. Roy Choudhury and Shail B. Jain, “Linear Integrated Circuits”, 3/e New Age International Publishers, ISBN 13: 9788122430981

Additional Materials

All material will be found on Google class room of this subject.

ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:
For Theory:

Assignments	20 % of 60 marks(week3,6,9,13)	Derivations , Numericals (Design & Analysis) and explanation (Diagram Operation)
Quiz	15 % of 60 (week 5)	MCQ
Attendance	15 % of 60 (week 9)	minimum 80
Mid semester (closed book)	50 % of 60 (due in week 10)	All the above
Final exam (closed book)	100% of 40 marks	All the Above

For Practical

Performance on Practical work	20% of 60 Marks	Assessment is based practical performance. Regularities ,accuracy and speed are the major parameters to be observed. Minimum 10 experiment is to be performed with the approval of faculty for appearing at practical exam.
Mini Project(Minor 1& Minor 2)	60 % of 60 Marks (7.5 Marks each for Design, Simulation, Breadboard implementation and GPB.)	Student has to gone through four stages. Design, Simulation, testing Using Bread Board and final on General Purpose board.

Attendance	20% of 60 marks	100 % attendance in Practicals
Final exam (Practical Exam)	100 % of 40 Marks	Final exam consists of two. One is Viva Voce of 30% and 30 % of Practical performance at the time of exam.

SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in mid semester or end semester will be considered for supplementary assessment in the respective components (i.e mid semester or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (mid semester or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of 2% of the maximum mark per calendar day

Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

Retention of Written Work

Written assessment work will be retained by the Course coordinator/lecturer for two weeks after marking to be collected by the students.

University and Faculty Policies

Students should make themselves aware of the University and/or Faculty Policies regarding plagiarism, special consideration, supplementary examinations and other educational issues and student matters.

Plagiarism - Plagiarism is not acceptable and may result in the imposition of severe penalties. Plagiarism is the use of another person's work, or idea, as if it is his or her own

- if you have any doubts at all on what constitutes plagiarism, please consult your Course coordinator or lecturer. Plagiarism will be penalized severely.

Do not copy the work of other students.
Do not share your work with other students (except where required for a group activity or assessment)

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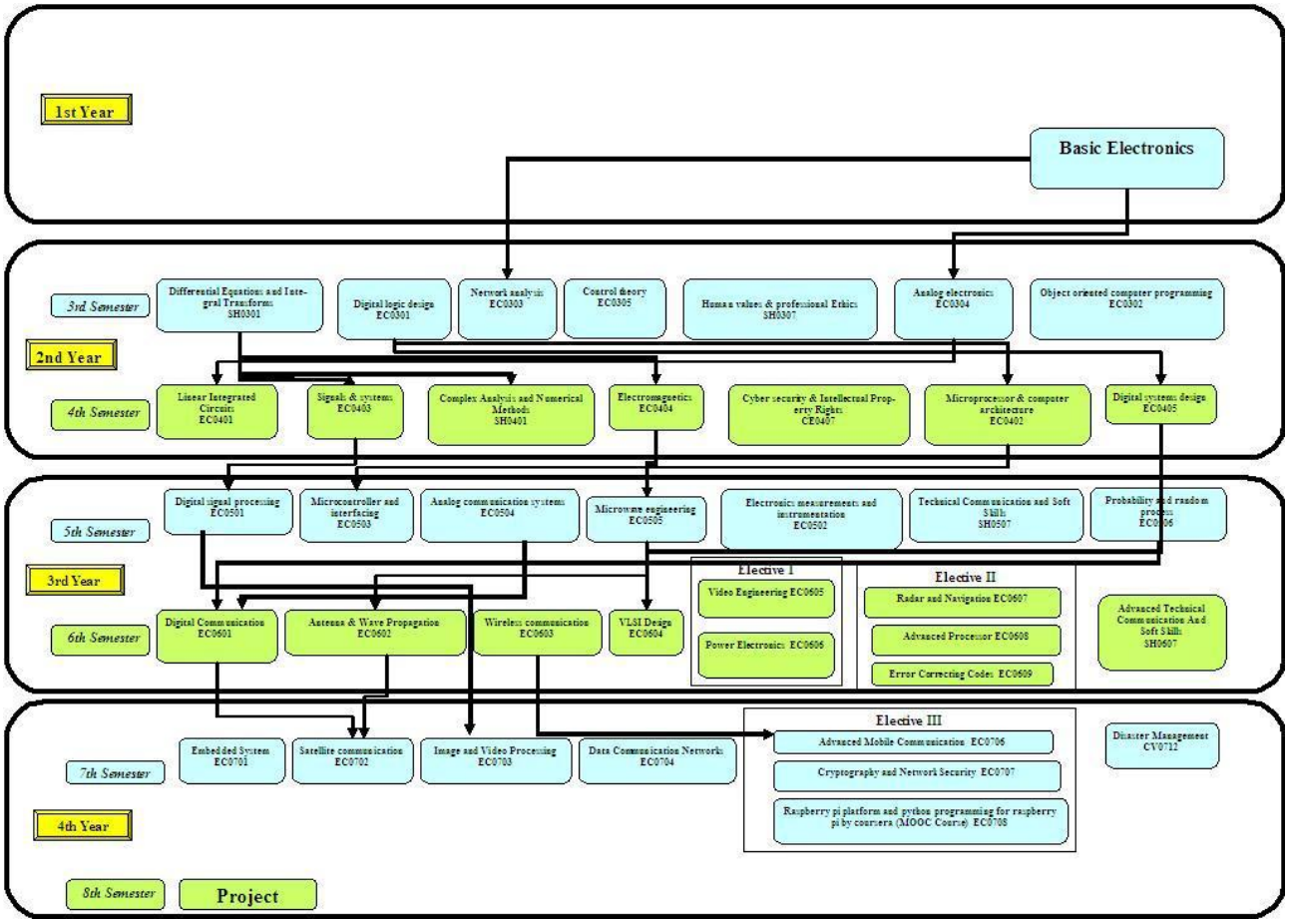
Course schedule(subject to change)

(Mention quiz, assignment submission, breaksetcas well in the table under the Teaching Learning Activity Column)

	Week #	Topic & contents	CO Addressed	Teaching Learning Activity (TLA)
	Weeks 1	Unit 1 mentioned in the syllabus	1 2	
	Weeks 2	Unit 1 mentioned in the syllabus	1 2	Assignment 1
	Week 3	Unit 1 mentioned in the syllabus	*1 2 3*	
	Week 4	Unit 2 mentioned in the syllabus	2 3	Assignment 1 submission and assignment 2 given, Test
	Week 5	Unit 2 mentioned in the syllabus	2 3 4	
	Week 6	Unit 2 mentioned in the syllabus	*2 3 4*	*Assignment 3 given and Assignment 2 submission*
	Week 7	Unit 3 mentioned in the syllabus	3 4	Quiz
	Week 8	Unit 3 mentioned in the syllabus	3 4 5	Assignment 4 given and Assignment 3 submission
	Week 9	Unit 3 mentioned in the syllabus	*3 4 5*	*Oral Test*
	Week 10	Unit 4 mentioned in the syllabus	3 4 5	Assignment 4 submission
	Week 11	Unit 4 mentioned in the syllabus	3 4 5	Query and problem solving
	Week 12	Unit 4 mentioned in the syllabus	3 4 5	Final Assessment declaration.

Prgram Map for Engineering
(Electronics and Communication)



Name of Institute: Institute of Technology and Engineering
Name of Faculty: Asst. Prof Abhishek Vaghela

Course code:
Course name: Microprocessor and Microcontroller
Pre-requisites: Digital Electronics, Microprocessor and Computer Architecture
Credit points: 4
Offered Semester: IV

Course coordinator (weeks 12)
Full name: Asst. Prof. Abhishek Vaghela
Department with siting location: EC Department, Signal Processing and Simulation Lab (Lab – 6)
Telephone: 3204
Email: abhishekvaghela.ec@indusuni.ac.in
Consultation times: Monday – Friday (4:00 PM to 4: 50 PM)

Course lecturer (weeks 12)
Full name: Asst. Prof. Abhishek Vaghela
Department with siting location: EC Department, Signal Processing and Simulation Lab (Lab – 6)
Telephone: 3204
Email: abhishekvaghela.ec@indusuni.ac.in
Consultation times: Monday – Friday (4:00 PM to 4: 50 PM)

Students will be contacted throughout the session via mail with important information relating to this course.

Course Objectives

By participating in and understanding all facets of this course a student will:

1) To introduce students to the architecture and operation of microprocessor & microcontrollers.
2) To familiarize students with programming of microcontroller.
3) To Introduce students to Embedded C programming
4) To familiarize students to interface various peripherals to the microcontroller.
5) To provide a strong foundation for designing real world applications using microcontroller.

Course Outcomes (CO)

1) Asses and solve basic binary math operations using microcontroller.
2) Apply knowledge and demonstrate programming proficiency using various addressing modes and data transfer instructions of the target microcontroller.
3) Compare accepted standards and guidelines to select appropriate microcontroller to meet the specified performance requirement.
4) Analyse assembly and C language programs of a microcontroller
5) Design electrical circuitry for interfacing various peripherals to the microcontroller.
6) Evaluate assembly and C language programs and download the machine code that will provide solutions to the real-world problems.

Course Outline

Unit	Contents	Total Hours
1	**Microprocessor Based Systems:** Microprocessor, Microcontroller, Von Neumann and Harvard Architecture, CISC and RISC Processors **8085 Microprocessor:** Architectural Block Diagram, Pin diagrams, Pin functions, Bus Organization, Internal operations and registers, Instruction set of 8085 processor	**10**
2	**8051 Microcontroller architecture:** Introduction to MCS -51 Family microcontrollers, Architectural block Diagram, Pin diagram, General Purpose and Special Function Registers, , Oscillator and clock circuit, Reset circuit, I/O Port circuits, Memory organization, Internal program and data memory, Introduction to program development tools **8051 Assembly language instructions :** Programming model of 8051, Addressing modes, data transfer instructions, I/O Port programming, Arithmetic and Logical instructions, Bit level instructions, Branching instructions (Jump and loop Jump and call), Concept of stack, subroutine and related instructions. **8051 Programming in C:Data types in 8051 C:** programming for time delay, I/O programming in 8051 C, Logic operations in 8051 C, Control statements and loops in embedded C, Functions and Arrays in	**10**

	embedded C, Data conversion programs in 8051 C, , Accessing code ROM space using 8051 C.	
3	**8051 Timer/Counter and Programming:** Use of counter as timer, Timer/Counters and associated registers, Various modes of timer/counter operations, Time delay programs in Assembly language/ Embedded C. **8051 Serial Port and Programming:** Basics of serial communication, RS232 standards, 8051 connection to RS232, Serial data input/output and associated registers, Various modes of serial data communication, serial data communication programs in Assembly language/ Embedded C **8051 Interrupts: Concept of Interrupt:** interrupt versus polling, Types of interrupts in 8051, Reset, interrupt control and associated registers, interrupt vectors, Interrupt execution, RETI instruction, software generated interrupt, interrupt handler subroutine for timer/counter and serial data transmission/reception in Assembly language/ Embedded C	**10**
4	**Applications and design of microcontroller based systems:** Interfacing of LEDs, 7 Segment display device, LCD display, DIP Switches, Push Button switches, Interfacing A/D converter, D/A converter, Relay, opto isolator stepper motor and DC motor **Introduction to ARM Cortex-M processor:** Cortex- M processor family, Advantages of the Cortex-M processors, Applications of the ARM Cortex-M processors, Architecture of Cortex - M processor, Introduction to Instruction set and programming of ARM Cortex-M processor	**10**

Method of delivery

Lectures
Laboratories

Study time

3 Hour’s theory and 2 Hour’s Practical session per week

CO-PO Mapping (PO: Program Outcomes)

CO/PO	PO											
	1	2	3	4	5	6	7	8	9	10	11	12
1	√					√	√	√				
2	√					√	√	√				
3		√		√						√		
4		√		√						√		
5	√		√	√								

Blooms Taxonomy and Knowledge retention (For reference)

(Blooms taxonomy has been given for reference)

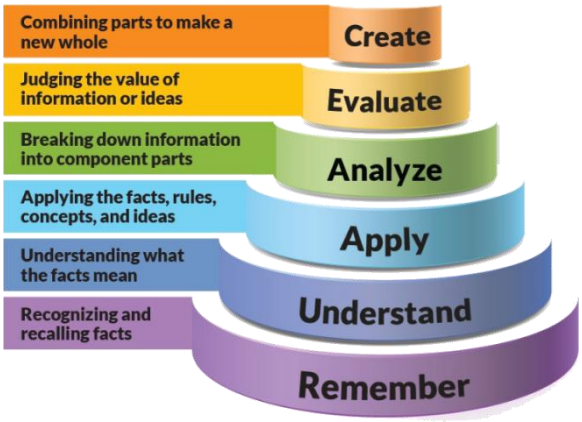


Figure 1: Blooms Taxonomy

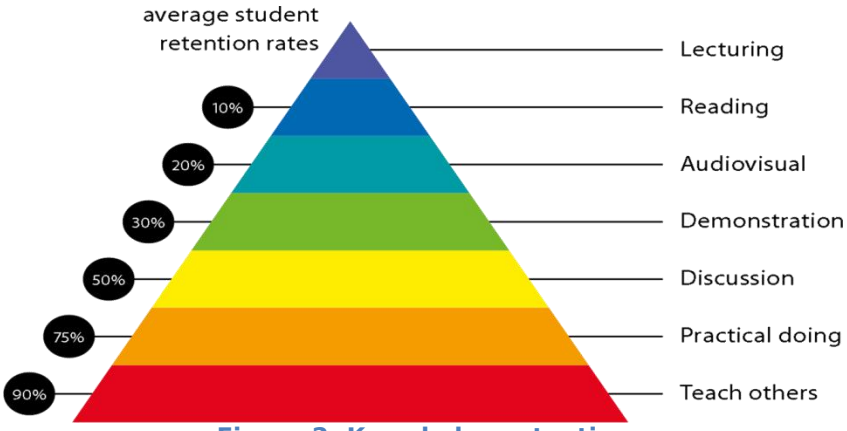


Figure 2: Knowledge retention

Graduate Qualities and Capabilities covered

(Qualities graduates harness crediting this Course)

General Graduate Qualities	Specific Department of Electronics and Communication Engineering Graduate Capabilities
Informed Have a sound knowledge of an area of study or profession and understand its current issues, locally and internationally. Know how to apply this knowledge. Understand how an area of study has developed and how it relates to other areas.	**1 Professional knowledge, grounding & awareness**
Independent learners Engage with new ideas and ways of thinking and critically analyze issues. Seek to extend knowledge through ongoing research, enquiry and reflection. Find and evaluate information, using a variety of sources and technologies. Acknowledge the work and ideas of others.	**2 Information literacy, gathering & processing**
Problem solvers Take on challenges and opportunities. Apply creative, logical and critical thinking skills to respond effectively. Make and implement decisions. Be flexible, thorough, innovative and aim for high standards.	**4 Problem solving skills**
Effective communicators Articulate ideas and convey them effectively using a range of media. Work collaboratively and engage with people in different settings. Recognize how culture can shape communication.	**5 Written communication** **6 Oral communication** **7 Teamwork**
Responsible Understand how decisions can affect others and make ethically informed choices. Appreciate and respect diversity. Act with integrity as part of local, national, global and professional communities.	**10 Sustainability, societal & environmental impact**

Practical work:

Sr.No	Title	Learning Outcomes
1	Introduction to IDE and Assembler directives.	Able to use keil IDE for ALP programming
2	8051 Assembly language programming for addition, subtraction, multiplication and division of two 8-bit numbers .	Able to write assembly language programs of 8051 in keil , able to use Keil IDE
3	8051 Assembly language programming for block data transfer between internal and external memory including overlapping blocks.	Able to write assembly language programs of 8051 in keil , able to use Keil IDE
4	8051 Assembly language programming using Arithmetic instructions	Able to write assembly language programs of 8051 in keil , able to use Keil IDE
5	8051 Assembly language programming using Logical Instructions	Able to write assembly language programs of 8051 in keil , able to use Keil IDE
6	8051 Assembly language programming for code conversions	Able to write assembly language programs of 8051 in keil , able to use Keil IDE
7	8051 Assembly language programming for Timers in different modes.	Able to use timer of 8051 microcontroller
8	I/O port programming in embedded C.	Able to Write embedded c code for I/O port
9	Timers and Counters programming in embedded C for time delay and frequency measurement using ISRs.	Able to write embedded c code for timers and counter
10	Digital clock programming using 7- segment display in embedded C.	Able to interface 7 segment write embedded c code for interfacing 7 segment display.
11	Programming of LCD in embedded C.	Able to interface LCD and write embedded c code for LCD
12	Serial communication and UART programming in Embedded C.	Able to write embedded c code for UART

Lecture/tutorial times

(Give lecture times in the format below)

Attendance Requirements

The University norms states that it is the responsibility of students to attend all lectures, tutorials, seminars and practical work as stipulated in the course outline. Minimum attendance requirement as per university norms is compulsory for being eligible for semester examinations.

Details of referencing system to be used in written work

Text books

1. Microprocessor Architecture, Programming, and Applications with the 8085, By Romesh Gaonkar, Penram International Publishing (India) LTD.

2. The 8051 Microcontroller and Embedded Systems Using Assembly and C, 2/e by Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin McKinlay (Second Edition , Pearson Education)

3. The Definitive Guide to ARM® Cortex®-M3 and Cortex®-M4 Processors, by Joseph Yiu, Publisher: Elsevier, ISBN: 9789351071754, 9351071758

Reference Books:

1. The 8051 Microcontroller & Embedded Systems using Assembly and C By K. J. Ayala, D. V. Gadre (Cengage Learning , India Edition).

2. Using the MCS-51 Microcontrollers By Han Way Huang Oxford Uni Press

3. Programming and Customizing the 8051 Microcontroller by Myke Predko Tata Mcgraw Hill.

Additional Materials

1. Microcontroller Course (http://nptel.ac.in/courses/Webcoursecontents/IITKANPUR/microcontrollers/micro/ui/TOC.htm)

ASSESSMENT GUIDELINES

Your final course mark will be calculated from the following:

Example:

Mid Semester Exam	40%
Attendance	**5%**
Simulation Project	10%
Assignment	5%
Final exam (*closed book*)	40%

SUPPLEMENTARY ASSESSMENT

Students who receive an overall mark less than 40% in internal component or less than 40% in the end semester will be considered for supplementary assessment in the respective components (i.e internal component or end semester) of semester concerned. Students must make themselves available during the supplementary examination period to take up the respective components (internal component or end semester) and need to obtain the required minimum 40% marks to clear the concerned components.

Practical Work Report/Laboratory Report:

A report on the practical work is due the subsequent week after completion of the class by each group.

Late Work

Late assignments will not be accepted without supporting documentation. Late submission of the reports will result in a deduction of -% of the maximum mark per calendar day

Format

All assignments must be presented in a neat, legible format with all information sources correctly referenced. **Assignment material handed in throughout the session that is not neat and legible will not be marked and will be returned to the student.**

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Do not share your work with other students (except where required for a group activity or assessment).

Course schedule (subject to change)

(Mention quiz, assignment submission, breaks etc as well in the table under the Teaching Learning Activity Column)

	Week #	Topic & contents	CO Addressed	Teaching Learning Activity (TLA)
	Weeks 1	Introduction to Microprocessor based systems, 8085 architecture , pin functions of 8085	CO1,CO2	BB,PPT
	Weeks 2	Instruction set of 8085	CO1,CO2	BB,PPT
	Week 3	Introduction to 8051 microcontroller, it architecture, Registers, Memory organization	CO2,CO3	BB,PPT
	Week 4	Instruction set of 8051, addressing modes of 8051	CO3,CO1,CO2	BB,PPT
	Week 5	Embedded C programming of 8051	CO3,CO4,CO5	BB,PPT

	Week 6	Timer / Counter programming of 8051 in assembly and C	CO3,CO4,CO5	BB,PPT
	Week 7	Serial port programming of 8051 in assembly and C	CO3,CO4,CO5	BB,PPT
	Week 8	Interrupt programming of 8051 in assembly and C	CO3,CO4,CO5	BB,PPT
	Week 9	Interfacing of Peripherals such as LED, Switch, 7 Segment Display and LCD	CO4,CO5,CO6	BB,PPT
	Week 10	Interfacing of A/D and D/A Converter, DC Motor and Stepper motor interfacing	CO5,CO6	BB,PPT
	Week 11	Introduction to Cortex-M family, Advantages of Cortex-M, Application of ARM Cortex-M processor	C01,CO2,CO3	BB,PPT
	Week 12	Architecture of Cortex - M processor, Introduction to Instruction set and programming of ARM Cortex-M processor	CO3,CO4,CO5	BB,PPT

ज्ञानेन प्रकाशते जगत्
INDUS UNIVERSITY